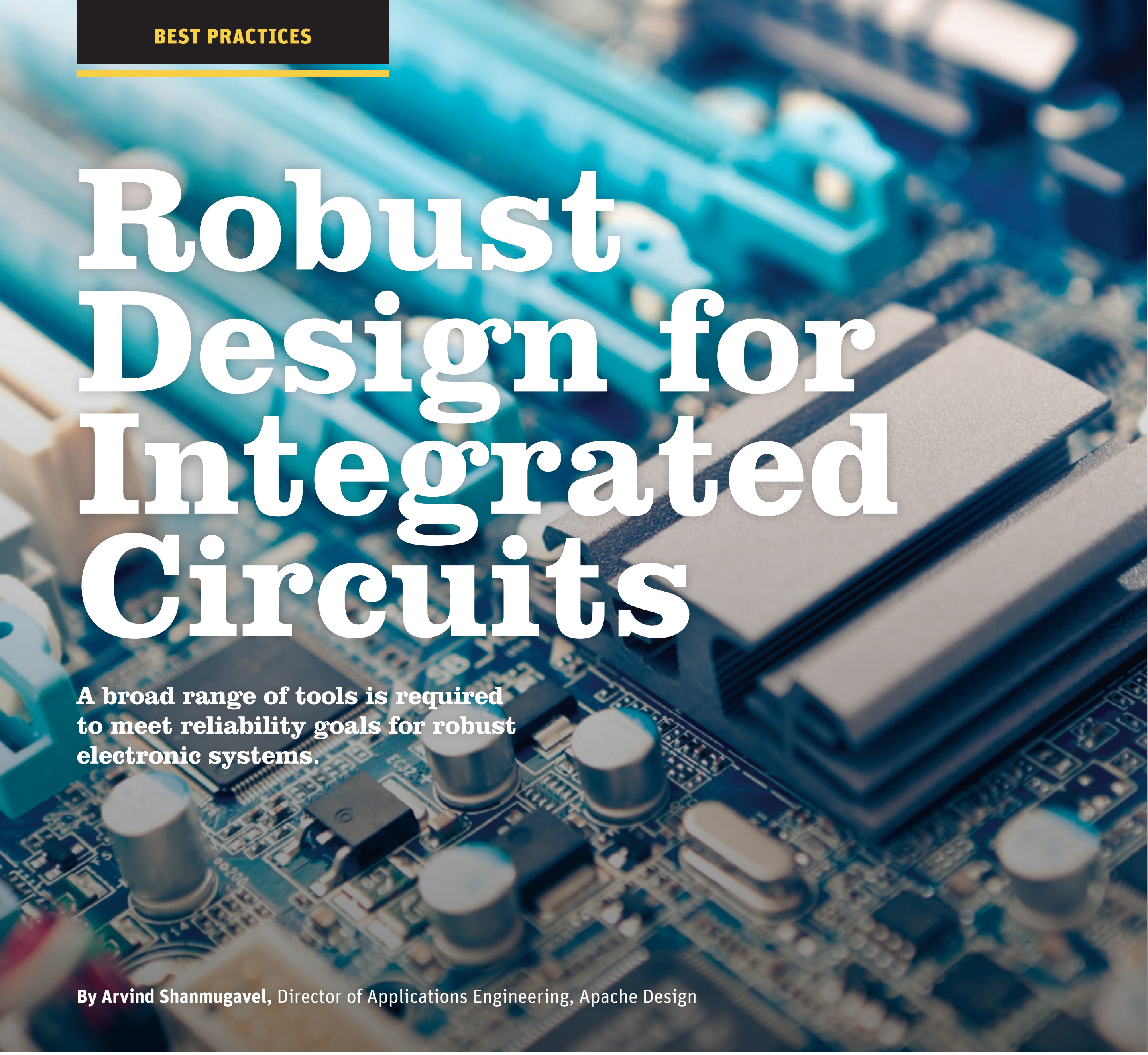


Robust Design for Integrated Circuits

A broad range of tools is required to meet reliability goals for robust electronic systems.

By Arvind Shanmugavel, Director of Applications Engineering, Apache Design

Designing robust electronic systems requires a multi-step approach with emphasis on reliability simulations. High-performance integrated circuits (ICs) are the workhorses of today's electronics industry. Designers must pay special attention to verifying these ICs for several operating and stress conditions to deliver a robust electronic system. Simulations such as supply noise coupling, thermal impact on electromigration (EM), electromagnetic interference (EMI) and electrostatic discharge (ESD) are key aspects of IC reliability verification.

As consumer electronics and mobile industries attempt to integrate ICs with greater functionality and higher speeds into smaller form factors, multiphysics simulation is key to capturing failure mechanisms. The automotive industry incorporates more and more electronic components in onboard safety and infotainment systems, mandating complex reliability verifications for ICs. No matter the application — from low-cost commodity ICs to high-lifetime and reliability ICs — there is a common theme of verifying complex failure mechanisms to meet product reliability goals.

INDUSTRY TRANSFORMATION

The IC industry has undergone a dramatic transformation in the past decade. Integrating complex functional modules, such as processor cores, intellectual property (IP) and high-speed I/O subsystems, has grown more common in IC designs. Performance, form factor and lower power are the driving forces behind IC integration in the mobile industry. On one hand, electronics product developers take a system-on-chip (SoC) design

Multiphysics simulation is key to capturing failure mechanisms.

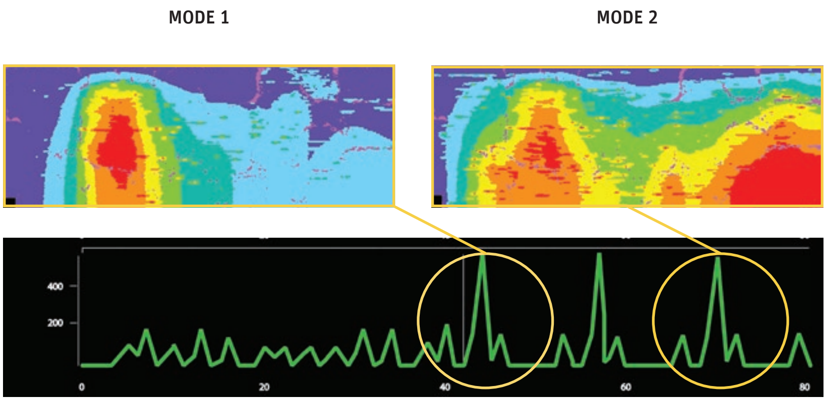
approach to fulfill the need for complex functions and operating modes within a limited area of an IC. On the other hand, semiconductor foundries migrate to smaller technology nodes for tighter integration of transistors in a smaller area. The most radical change seen in this market segment is the move from bulk to multigate 3-D-FinFET transistors in advanced process nodes. FinFET transistors provide the unique advantage of lower leakage power with higher operating speeds, compared to planar transistors.

Another trend is integrating multiple ICs within the same package. The next decade will see further evolution: the integration of 3-D–ICs using through-silicon vias (TSVs), interposers and advanced packaging techniques. Lower power, higher bandwidth and form factor requirements are the main factors driving this transformation of ICs into 3-D–IC subsystems.

Just as the IC industry is embracing new transistor architectures, SoC integration and 3-D–IC packaging techniques, the simulation industry must keep up with complex verification needs. Failure analysis and reliability simulation needs to incorporate new multiphysics approaches for solving chip, package and system cosimulation challenges. Complex failure mechanisms must be simulated, including thermal failure, thermal-induced EM, EMI between ICs, and ESD in a multi-IC package.

MARKET REQUIREMENTS

Reliability verification standards typically are dictated by the end use of an IC in a specific market. Consumer electronics and the mobile industry are by far the largest markets for ICs by volume. The smartphone sector integrates various high-end ICs, such as wireless modems, application processors, memory chips, GPS modules, CMOS image sensors and touch-screen controllers — all in an extremely small form factor. These IC components must perform reliably by themselves as well as in the context of the system. Typically, ICs inside a smartphone system must meet strict guidelines for lifetime reliability verification, ESD and EMI. Since smartphones are predominantly software application driven, different types of applications can dictate the reliability metric. For example, thermal reliability must be performed using



▲ Chip dynamic voltage drop based on two different operating modes

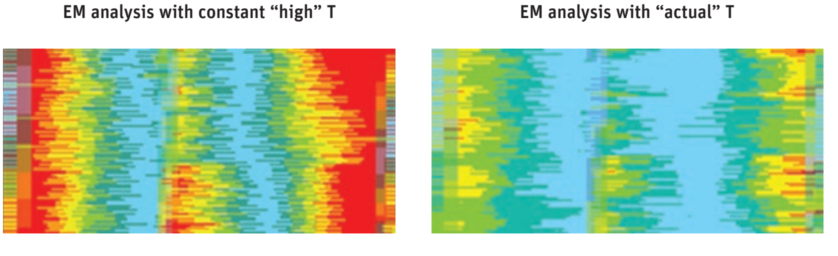
high activity modes with multiple wireless and GPS modules all operating at the same time. Conversely, lifetime reliability must be performed with the impact of the modes of operation through a three- to five-year lifetime.

In automotive, defense and aerospace industries, product reliability is highly important, often trumping the need for complex functionality. Mission-critical applications, such as safety systems in an automobile or fly-by-wire systems in aeronautics control, require electronic components that can tolerate extreme temperatures and constant electromagnetic interference, as well as operate throughout the system's entire lifespan. These systems have special reliability metrics for electronic components and may require meeting MIL-STD specifications. Typically, ESD and EMI standards are much higher than those for consumer-grade electronics for safety systems. EM checks are performed to meet a typical 10- to 15-year lifespan, compared to three to seven years for consumer-grade electronics. Thermal standards for these ICs are typically checked between –55 C and +175 C to meet high-temperature operating lifetime (HTOL) metrics.

RELIABILITY METRICS FOR ICS

Electromigration and Thermal Reliability

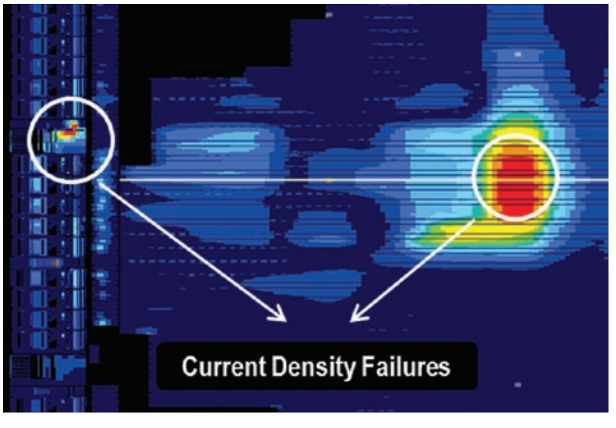
EM is a well-known lifetime failure mechanism in the IC industry, represented by mean time to failure (MTTF), as defined by Black's equation [1]. Every IC designed today must be verified for EM failures for a specific product lifetime. Previously, EM checks were performed with worst-case operating conditions, typically including the highest activity for the device coupled with the worst-case operating temperature. However, with today's compressed IC design cycle, designers no longer have the luxury of designing for the worst-case scenario.



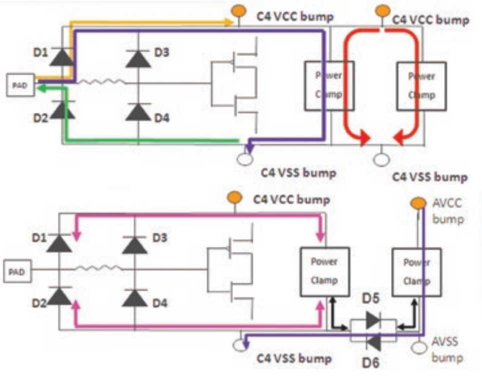
▲ Thermal feedback for electromigration analysis

Most smart ICs run some form of firmware or software, depending on the end use. The type of software application being run directly dictates the amount of activity that will be generated on the IC. Understanding the application-generated activity throughout the lifetime of the device is important for verifying EM failures. Consider the example of an application processor in a smartphone: The processor can transition between multiple operating modes such as video encoding, audio playback, GPS usage, call answer or sleep mode. Each application has a different activity factor generated on the IC. Each operating mode will use only a certain percentage of lifetime for the device. Understanding the activity factor for each mode of operation and the percentage of its use during the lifetime is important in performing EM simulations for the power, ground and signal nets. Designing the IC with an always-on high activity mode can lead to overdesigning the chip, which takes up valuable metallization resources that could be used elsewhere. To avoid this situation, using application-aware reliability modeling is a must for designing today's ICs.

The thermal impact on EM is another important aspect of reliability. The maximum EM limit for a metal wire in an IC decreases exponentially as temperature increases. Verifying EM for an IC at the correct operating temperature can help to drastically reduce the number of true EM violations that must be addressed. Understanding the temperature gradient of an IC at a micron resolution is necessary for accurate reliability predictions. An IC's end application also needs to be considered during thermal-driven EM analysis. For mission-critical applications, worst-case operating temperatures are typically used for design sign-off. However, for mobile and consumer-grade electronics, an accurate spatial distribution of the temperature is generally used.



▲ Current density check during an ESD event. Highlighted areas in red indicate the points of metal failure.



▲ Complex ESD pathway modeling for a typical IC. Every path highlighted should be checked against a resistance limit.

Electrostatic Discharge

ESD is the transfer of charge from one body to another, resulting in a large flow of current. An ESD event on an IC can inadvertently increase the voltage of the signal or power net beyond the device's breakdown voltage, ultimately rendering the IC useless. To protect operating devices from reaching high voltages, ESD protection devices are usually placed near I/O connectors, providing a low-impedance path for the ESD current to shunt the charge from reaching the operating devices. Utilizing a systematic simulation-based solution is necessary to carefully optimize these protection devices and verify proper ESD margins.

The ESD design margin is the voltage range above the normal operation of the IC but below the breakdown voltage of the specific process technology. This is typically the voltage range in which ESD protection devices operate to protect the IC from breakdown. As ICs move toward smaller technology nodes with lower breakdown voltage characteristics, the ESD design margin is drastically decreased, and the metal burnout characteristics are decreased as well. Re-using an ESD protection scheme designed in an earlier technology node can no longer be done in subsequent nodes. With die area at a premium and design margins shrinking, ESD schemes need to be designed with a systematic simulation-driven approach, placing protection devices at appropriate locations without overdesigning. Additionally, interconnect geometries must be verified against burnout during an ESD event by performing current density checks.

SoC integration with multiple cores and mixed-signal modules increases the complexity of ESD verification. Each core or module potentially can have its own power/ground network. Typically, an ESD pathway can be between any pair of power, ground or signal pin combinations. With the large number of power/ground domains in SoCs, protection devices must be placed between all possible combinations of power and ground nets to account for complex discharge pathways. Three-D–IC architectures pose a unique challenge in validating ESD. This type of IC has two or more dice in the same package module, so ESD pathway modeling needs to account for multi-die simulations when performing checks.

Electromagnetic Interference

EMI is caused when the electromagnetic field from one IC coupled with the metal geometries on the system interferes with the operation of a neighboring IC in the system. The failure mode of EMI is very difficult to model in electronic systems; however, electromagnetic radiation emitted by an IC coupled with the metal interconnects of the system can be modeled and simulated with a complete chip–package–system approach.

Using 3-D full-wave electromagnetic modeling tools for the package and board, along with proper current signatures for the die, a user can accurately simulate the amount of near- and far-field radiation emitted by an IC subsystem. Typically, near- and far-field radiation patterns are simulated for multiple IC operating modes in the electronics system. EMI filter design and placement is usually done to filter out specific radiation spectrums and protect against electromagnetic coupling. Safety systems in automotive and aeronautics applications are commonly analyzed under varying load and ambient conditions for EMI before they are assembled in the system.

FROM CHIP TO SYSTEM

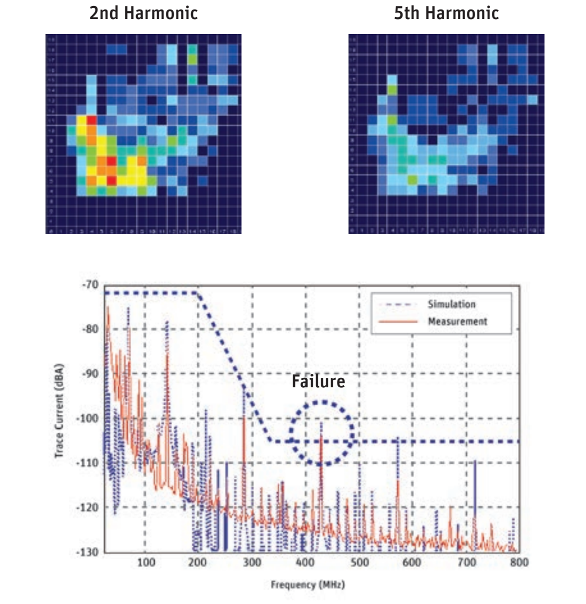
Any electronic system consists of multiple ICs integrated on the same board or product. To ensure the robustness of a product, ICs need to be verified within the context of the electronic system. Additionally, the electronic system needs to be validated with the impact of the various ICs in their respective operating conditions. Chip-aware system design and system-aware chip design approaches are imperative due to complex failure mechanisms. A seamless model hand-off between IC and system designers is necessary to manage complex reliability simulations.

A chip-aware system design requires accurate IC models with a common reference point to be used in systems-level verifications. For example, a chip power model (CPM) of an IC with accurate impedance and current profiles is needed to verify proper electronic behavior of the system. Tools such as ANSYS SIwave and Sentinel-PSI can use a CPM model to perform system-level EMI verification. Similarly, a chip thermal model (CTM) of an IC is required to accurately predict thermal behavior of the system. Platforms such as Sentinel-TI and ANSYS Icepak can use a CTM to perform accurate thermal reliability simulations.

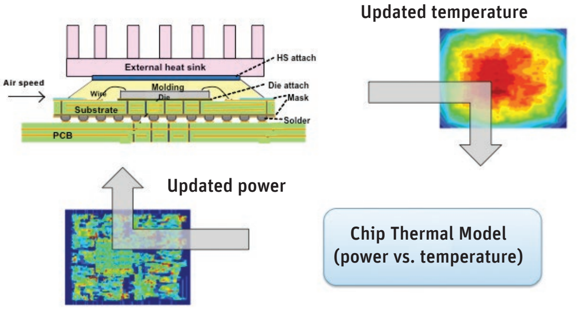
A robust system-aware chip design requires accurate modeling of the IC packages and circuit boards while performing die-level simulations. For example, an S-parameter model or electrical network of the package is needed to perform die-level transient voltage drop or ramp-up simulations. Tools such as ANSYS SIwave or Sentinel-PSI can create package models that can be used during a RedHawk transient simulation. Similarly, a die-thermal profile with micron resolution can be generated from Sentinel-TI to be used for accurate temperature-aware electromigration simulations of the die using RedHawk.

SIMULATION AND IC RELIABILITY

Predicting lifetime and understanding failure mechanisms are important to any IC design process. Simulation tools must offer capabilities to understand the various operating modes, ambient conditions and system interactions with the IC to accurately predict failure mechanisms. Reliability verification tools also need to keep up with evolving process technology manufacturing and 3-D packaging techniques. A robust electronic system can be developed only by checking the impact of the IC on the system as well as the impact of the system on the IC. A combined chip–package–system cosimulation environment that can predict these complex failure mechanisms is necessary. Advanced reliability simulation techniques with multiphysics simulation are an integral part in realizing the promise of a robust electronic system.



▲ Chip EMI map showing the 2nd and 5th harmonics. Failure highlighted when measurement exceeds the EMI limit.



▲ IC power thermal loop using a CTM inside Sentinel-TI; convergence of power and thermal required for accurate IC temperatures

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