# Fostering Thermal Design Innovation using Chip-Package-System Analysis Techniques

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## Challenges

As devices continue to become smaller and more portable Moore's law continues to increase the number of transistors that fit within a chip albeit many predict an end to this in the near future. However new interconnect technologies that use Through-Silicon-Vias (TSVs) can place ICs next to each other using 2.5D Interposers or stack chips in 3D resulting in even greater system scaling. This corresponds to non-digital functionalities that traditionally reside on printed circuit boards (PCBs) being migrated into a package or chip and has enabled the design community to begin "More than Moore"[i] where Moore refers to "Moore's Law."[ii]

This change where chips are being interconnected using 2.5D interposers or 3D stacking presents new challenges because it becomes increasingly difficult to operate within a devices thermal envelope. This makes accounting for thermal early in a design extremely important to the success of any product. Recent rumors indicate that the Galaxy S7 will include heat pipes to successfully remove heat improving the devices performance highlighting how important innovative thermal design is becoming.[iii,iv] Additionally the impact from just reducing silicon node size has placed great thermal burdens within traditional package sizes due to reduced trace-trace spacing and widths while maintaining the same amperage requirements. As the electronics industry continues evolving it requires improvements to existing CAD and simulation tools in support of these challenges.

ANSYS' latest release (R17) adds significant improvements in the area of predicting thermal responses for system design and doing so early in the design cycle of a product. These improvements start at the IC where Chip Thermal Models (CTM) are created using RedHawk which are then leveraged by Icepak which performs system level thermal analysis. SIwave adds Joule heating losses from the IC package and PCB into Icepak increasing the overall fidelity of the system model. Finally, the thermal response is passed to ANSYS Mechanical where thermal fracture, stress/strain, and warpage analyses are completed. These simulation software products provide end-to-end solutions for engineering organizations helping engineers across organizations from the architect to the system integrators. The remainder of this article will focus on the Joule Heating improvements made between SIwave and Icepak which enables more effective collaboration between electrical engineers (EEs) and mechanical engineers (MEs).

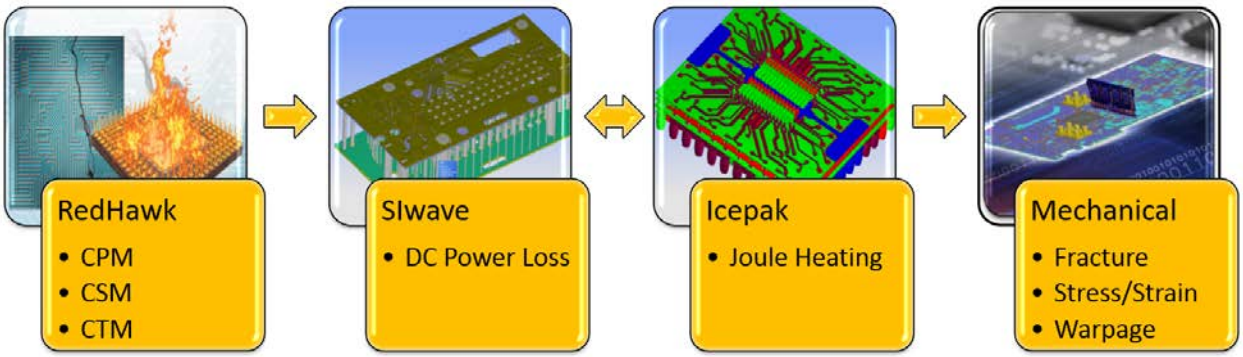


Figure 1: ANSYS Multi-physics solution from chip to product

## Joule Heating Solutions

Let's begin by quickly reviewing where SIwave and Icepak are generally deployed within an engineering organization. SIwave is often referred to as a, "Hybrid Field Solver"[v] and is predominantly utilized by EEs. SIwave performs AC & DC electrical analyses of electronic packages and PCBs as shown in Table 1.

| Functionality | SIwave – DC | SIwave – PI | SIwave |
|---|---|---|---|
| ECAD Translation | ✓ | ✓ | ✓ |
| SIwave & 3D Layout GUI | ✓ | ✓ | ✓ |
| $I^2R$ DC solver (Joule Heating with Icepak) | ✓ | ✓ | ✓ |
| DC Path Resistance Solver | ✓ | ✓ | ✓ |
| Plane Resonance Solver | | ✓ | ✓ |
| Automated Decoupling Analysis Optimization | | ✓ | ✓ |
| AC SYZ Solver | | ✓ | ✓ |
| AC Frequency Sweep Solver | | ✓ | ✓ |
| Synopsys HSPICE Integration | | ✓ | ✓ |
| $Z_o$ Scanner (Single Ended & Differential) | | | ✓ |
| Cross-talk Scanner | | | ✓ |
| TDR Wizard | | | ✓ |
| Near-Field EMI solver | | | ✓ |
| Far-Field EMI Solver | | | ✓ |
| Flight Time Signal Net Analyzer | | | ✓ |
| Circuit Analysis (IBIS, IBIS-AMI, .tran, .ac, …) | | | ✓ |
| Network Data Explorer & Macro-modeling | | | ✓ |
| Conducted & Radiated EMI with Circuits | | | ✓ |

Table 1: SIwave capability chart

Icepak is a CFD (computational fluid dynamics) solver that accounts for numerous types of flow and thermal conditions. It uses the ANSYS Fluent solver to provide accurate thermal temperatures for electronic products. Thermal engineers or MEs predominantly use Icepak to provide thermal solutions for devices ranging from cell phones and tablets to cellular base stations and data centers.

With the ANSYS R17 release new capabilities within these products enable EEs and MEs to collaborate very efficiently throughout an entire product life cycle starting with concept design all the way through manufacturing and reliability testing. The most significant improvement is around *Ease-of-Use* where an EE can perform real-time thermal analysis from the SIwave graphical user interface (GUI) to help identify design obstacles while promoting close collaboration between the architect, EE, ME and system integrator. The basic thermal analysis performed by an EE can be easily handed off to a thermal engineer

where greater detail can be added thereby solving thermal-electric design challenges together. A simple package example will be highlighted below.

The electronic package studied for this paper has the following characteristics: flip chip BGA package with 4 metal layers and is ~10 mm x 10 mm. There are 2 power planes and a single ground plane along with numerous signal traces. In Figure 3 the Vdd core power distribution network (PDN) is red, the Vdd 3.3V PDN is blue with Ground being green and signal nets being garnet.

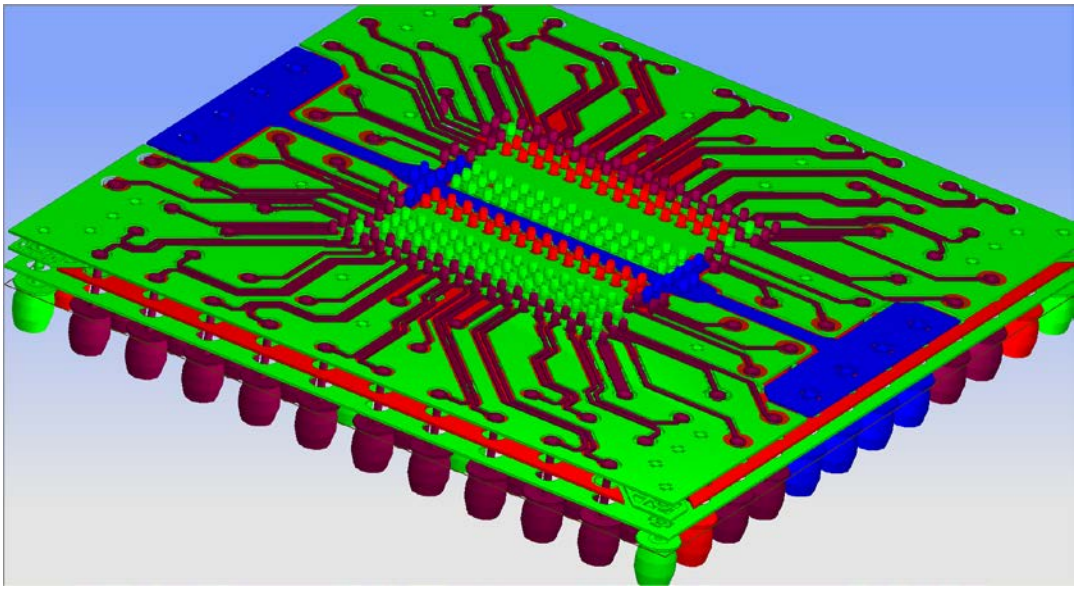

Figure 2: IC package analyzed for this article

For this analysis the authors assumed that the C4 bumps were divided into a 3x3 operating matrix where the Vdd, Vdd 3.3V and Ground bumps were grouped into different operating areas. This enables the engineers to make trade-offs between thermal considerations under different operating vectors while looking at ball out configurations and the impact each has on AC/DC inductance and resistance. Additionally, this has the added value that temperature effects due to Joule heating are accounted for. This particular design points out that regions 3:1, 3:2, and 3:3 have very few ground bumps which could lead to poor signal integrity for traces in those regions.

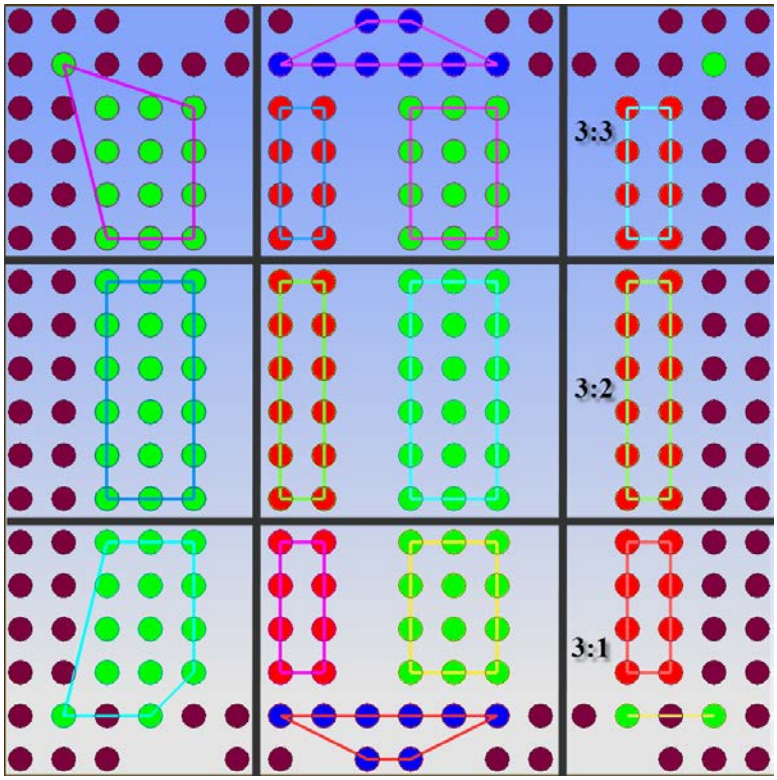


Figure 3: C4 ball out configuration with power and ground groupings

The method uses an iterative approach that leverages “Workflow Wizards” for easy setup and analysis. These wizards enable highly accurate results while ensuring a consistent and repeatable process that minimizes human setup errors.

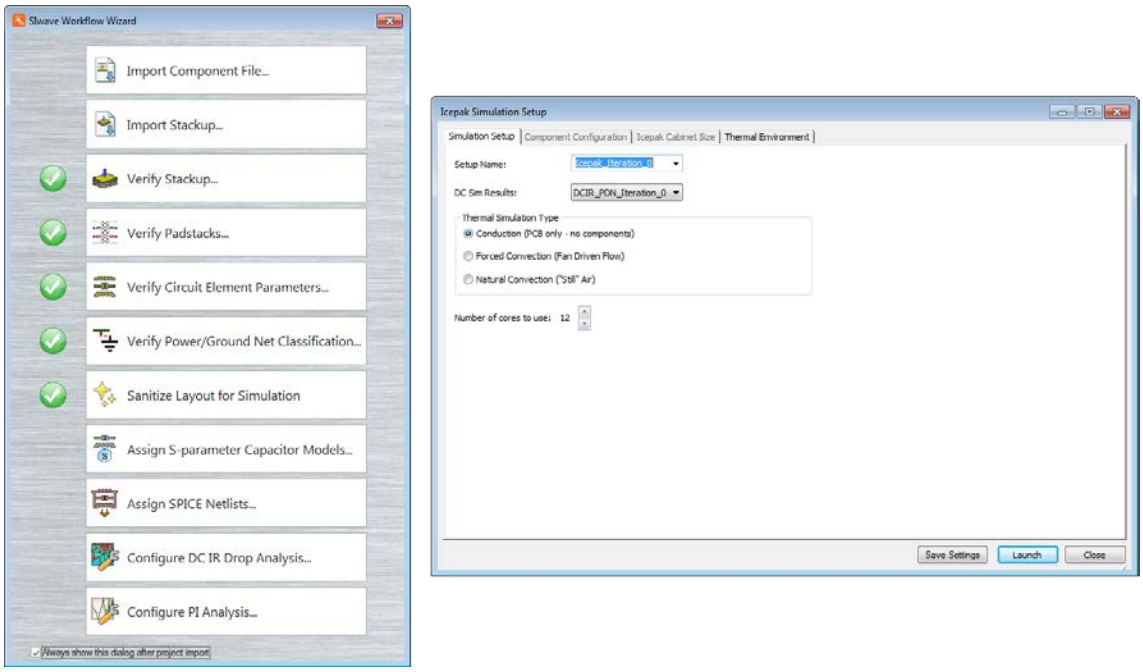


Figure 4: Workflow wizards that enable easy setups that are consistent, repeatable and accurate

This analysis focused on distributing approximately 20 amps of current within the Vdd PDN and approximately 10 amps within the Vdd 3.3V PDN assuming an ambient temperature of 20°C. This produces a fairly significant amount of power loss within the copper as shown in Table 2 below. With approximately a ½ watt of power loss within the copper the effect of Joule heating is quite significant. Engineers can leverage ANSYS DesignXplorer to perform Design of Experiment studies where parameters such as voltages, currents, operating vectors, stack up changes, ambient temperatures, geometry modifications … can be analyzed to understand system operation under varying conditions and corners.

| Iteration | DC Power Loss - Top Layer (W) | Joule Heating - Top Layer (°C) |
|---|---|---|
| 0 | 0.36 | 61.7 |
| 1 | 0.409 | 91.8 |
| 2 | 0.451 | 95.8 |
| 3 | 0.455 | 96.6 |

Table 2: Joule heating copper losses for the top metal layer within the package

The results from Iteration 3 are shown in Figure 6 where the voltage drop, current density, via currents, power loss per layer, and temperature rise is analyzed to predict product performance. It has been shown through the authors' experience that most systems converge to an accurate solution within 2-3 iterations.[vi] The direction of current flow is indicated by the directional arrow with the color providing the density where red indicates high density current flow. This produces results that are very easy to understand while pointing out problematic areas due to insufficient vias between metallized layers or due to copper floods that have been "Swiss Cheesed" due to via anti-pads. In this particular package it is easy to see the neck down of the Vdd 3.3V PDN near the center of the package.

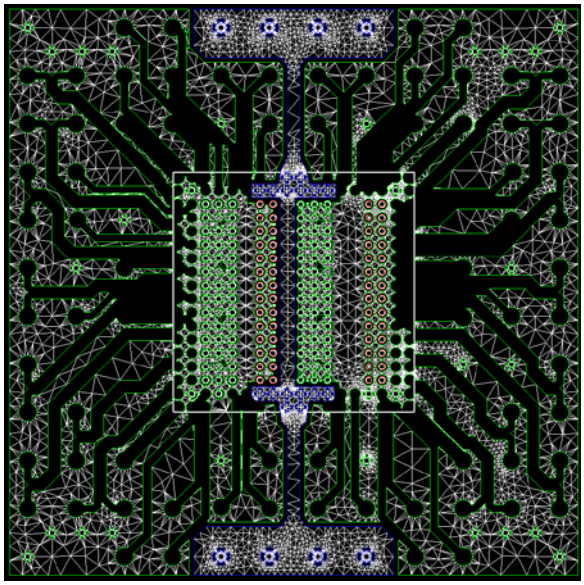

Figure 6a: Automatic & Adaptive Conformal Mesh

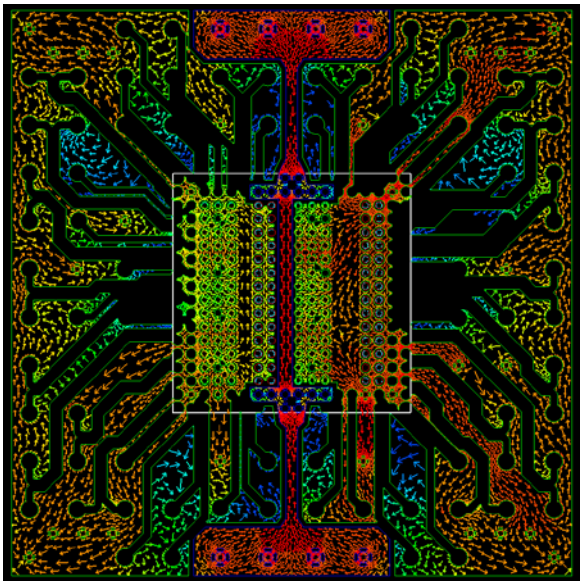

Figure 6b: DC Current Density – Top Layer

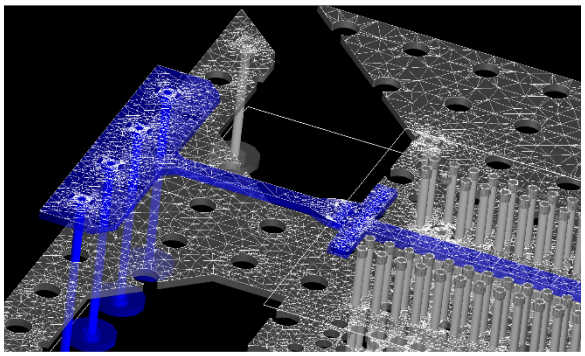

Figure 6c: Automatic & Adaptive Conformal Mesh

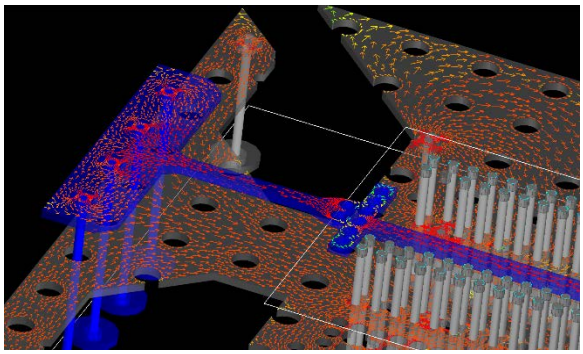

Figure 6d: DC Current Density – Top Layer

The solution produces highly accurate results due to ANSYS' proprietary automatic and adaptive meshing technique that continues to refine an object's mesh until the specified convergence criteria are met. The proprietary method is extremely fast while using minimal compute resources; for example, this package solved in 18 seconds with peak RAM usage of 263 MB. Once the electrical power losses have been solved for those losses automatically map into a conformal Icepak mesh where thermal boundary conditions are applied from the Icepak Simulation Setup Wizard shown in Figure 5. This enables a single engineer to quickly solve thermal-electric problems without sacrificing accuracy.

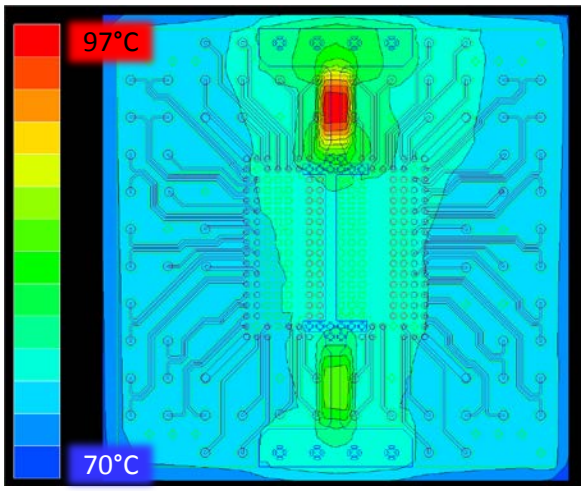


Figure 7a: PDN Temperature – Top Metal Layer

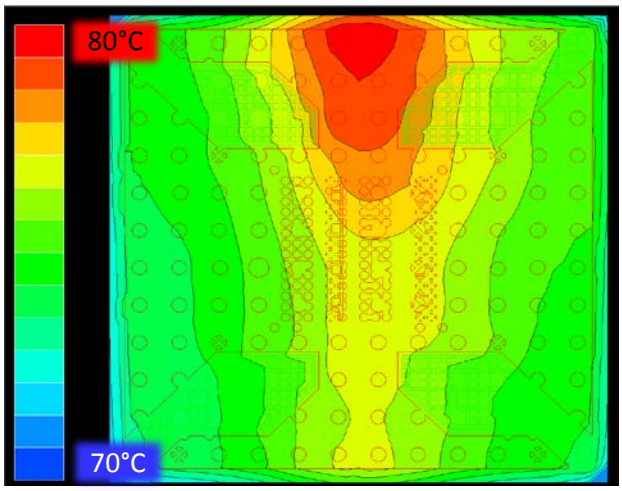


Figure 7b: PDN Temperature – 2nd Metal Layer

The key to collaboration is that each engineer can work within the graphical environment they are most familiar with while ensuring consistent and accurate setups are utilized. The EE can quickly update the ME about the impact that Joule Heating has within a product using the SIwave GUI while sending the automatically created Icepak .tzr project to the ME for deeper investigation.

## Conclusion

This article briefly discusses ANSYS R17 improvements where EEs and MEs can more effectively collaborate when designing electronic products. It shows how SIwave can invoke the Icepak solver to provide solutions when hitting thermal envelopes throughout all design areas of the product lifecycle.

Additional improvements that incorporate chip power delivery and mechanical design are briefly mentioned and readers are encouraged to review those developments on www.ansys.com.

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[i] http://www.tsmc.com/english/dedicatedFoundry/technology/mtm.htm

[ii] https://en.wikipedia.org/wiki/Moore%27s_law

[iii] http://www.technobuffalo.com/2015/12/07/galaxy-s7-samsung-engineer-defends-rumored-cooling-system/

[iv] http://wccftech.com/is-galaxy-s7-overheating-samsung-looking-for-heat-pipe-manufacturers-might-provide-some-evidence/

[v] S.G. Pytel, S.C. McMorrow, T. Dagostino, S. Polstyanko, W. Thiel, and R. Hall, "Successful Practices for the Modeling of Printed Circuit Boards and Substrates Using Electromagnetic Field Solvers", *43rd International Symposium on Microelectronics*, October 31 – November 4, 2010.

[vi] J.E. Bracken, S.V. Polstyanko, S.G. Pytel, and I. Waldron, "Coupled Thermal–Fluid–Electrical Simulation for Printed Circuit Board Design", *International Conference on Electromagnetics in Advanced Applications (ICEAA)*, Torino, Italy, September 12 – 17, 2011, pp 1005-1008.